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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,872	06/25/2003	John W. Marshall	112025-0516	3020

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EXAMINER	
NGUYEN, DUSTIN	
ART UNIT	PAPER NUMBER
2454	
MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/603,872	MARSHALL ET AL.	
	Examiner	Art Unit	
	DUSTIN NGUYEN	2454	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 May 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 13-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-11,13-16,18-26,28-32 and 34* is/are rejected.

7)☒ Claim(s) *6,17,27 and 33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-11 and 13-34 are presented for examination.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01/29/2009 has been entered.

Response to Arguments

3. Applicant's arguments filed 05/14/2009 have been fully considered but they are not persuasive.

4. As per remarks, Applicants argued that (1) Henderson does not suggest modifying packet header data.

5. As to point (1), Henderson discloses modifying packet header data [paragraphs 0005]. Specifically, Henderson shows the header and payload portions of the packet [Figure 4; and paragraph 0046], and discloses the editing operation added an MPLS field to the packet header [Figure 5; and paragraph 0047].

6. As per remarks, Applicants' argued that (2) Henderson fails to teach or suggest "performing ... the operations associated with the commands ... to modify the data ... while the data is transferred from the source to the destination".

7. As to point (2), the previous Office Action had addressed this remark/argument. As previously stated, Examiner respectfully disagrees since Henderson discloses a system and method for quickly modifying state information of packets [Abstract]. The system of Henderson includes a service processor coupled to Ethernet switch 106 for receiving and sending packets [Figure 1; and paragraph 0023], and the service processor 110 comprises a packet input unit 210 for receiving packets from Ethernet switch, an editing unit 216 and a packet output unit 222 for sending out packets. The editing unit receives edit instructions from the packet processing controller 200 and is responsible for packet editing which includes variety of packet modification functions such as inserting data in a packet, deleting data from a packet, etc ... [i.e. broadly interpreted as "performing ... the operations associated with the commands ... to modify the data" as claimed] [Figure 2; and paragraphs 0030-0034]. In addition, Henderson discloses each packet that arrives at a services processor is assigned a packet context

that contains information about the packet, state information related to the packet, and about the actions to be done to the packet, this context identifies the next action to be taken in processing the packet ... Information within the state tables is often modified in real time as packets are processed [i.e. broadly interpreted as "performing ... the operations associated with the commands ... to modified the data ... while the data is transferred from the source to the destination" as claimed] [paragraphs 0007 and 0008]. As such, the claims remain rejected as written, unpatentable over the cited prior art.

Allowable Subject Matter

8. Claims 6, 17, 27 and 33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English

language.

10. Claims 1, 13, 22 and 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Williams [US Patent No 7,031,325].

11. As per claim 1, Williams discloses the invention as claimed including a method for modifying packet header data transferred from a source to an output buffer [i.e. modifying or stripping VLAN header] [col 12, lines 12-17], the method comprising the steps of:

reading one or more instructions, by a processor, each instruction indicating an operation to modify the packet header data [i.e. the PVQ control logic decides how to handle the VLAN information associated with a data frame based on information in the untagged set and opcode fields] [Figure 6; col 9, lines 35-44; and col 10, lines 57-col 11, lines 11];

generating, in response to the one or more instructions, one or more commands wherein each command is associated with the operation to modify the packet header data [i.e. the PVQ control logic generates a new opcode in the forwarding descriptor] [770, Figure 7; col 9, lines 44-47; and col 11, lines 12-col 12, lines 2];

placing the commands in a data structure [i.e. transfers the forwarding descriptor with the new opcode to the appropriate queue] [770, Figure 7; and col 11, lines 66-col 12, lines 2];

initiating a transfer of the packet header data from the source to the output buffer [i.e. transfers [i.e. forward to dequeuing logic or transmitter 210] [210, 240, Figure 3; and col 9, lines 54-64]; and

performing, by a device operating independently of the processor, the operations associated with the one or more commands contained in the data structure to modify the packet

header data as directed by the one or more commands while the packet header data is being transferred from the source to the output buffer [i.e. the dequeuing logic may then perform any necessary modification to the data frame while it transfers the data frame into the transmit FIFO buffer] [780, 790, Figure 7; and col 12, lines 3-17].

12. As per claim 13, it is rejected for similar reasons as stated above in claim 1. Furthermore, Bremer discloses context memory configured to hold packet header data [Figures 2 and 3; and Abstract].

13. As per claims 22 and 28, they are rejected for similar reasons as stated above in claim 1.

14. Claims 1-4, 7, 9-11, 13-15, 18, 20-25, 28-31 and 34 are rejected under 35 U.S.C. 102(e) as being anticipated by Henderson et al. [US Patent Application No 2004/0042490].

15. As per claim 1, Henderson discloses the invention as claimed including a method for modifying packet header data transferred from a source to an output buffer [i.e. the packets often must be processed or modified between their source and destination] [paragraphs 0005 and 0007], the method comprising the steps of:

reading one or more instructions, by a processor [i.e. the table entry processor receives table entries retrieved by the packet processing controller] [paragraph 0026], each instruction

indicating an operation to modify the packet header data [i.e. packet modification functions, such as insert or delete data from packet] [paragraph 0034];

generating, in response to the one or more instructions, one or more commands [i.e. a code that specifies which editing operation will be performed] wherein each command is associated with the operation to modify the packet header data [i.e. insert operation, delete operation, etc…] [Figure 6; and paragraph 0049];

placing the commands in a data structure [i.e. store in edit registers] [Figure 6; and paragraphs 0049 and 0069];

initiating a transfer of the packet header data from the source to the output buffer [i.e. as packet is traversed] [paragraphs 0007, 0008, 0027 and 0039]; and

performing, by a device operating independently of the processor, the operations associated with the one or more commands contained in the data structure to modify the packet header data as directed by the one or more commands while the packet header data is being transferred from the source to the output buffer [i.e. the editing unit to apply the editing operations] [216, Figure 2; and paragraphs 0034, 0036 and 0069].

16. As per claim 2, Henderson discloses acquiring the packet header data from the source [i.e. packet input unit] [210, Figure 2; and paragraph 0030].

17. As per claim 3, Henderson discloses generating a bit mask associated with the acquired packet header data; and transferring the bit mask and the acquired packet header data to the output buffer [i.e. mask multiplexer] [Figure 11; and paragraph 0081].

18. As per claim 4, Henderson discloses wherein the data structure comprises one or more entries wherein each entry is associated with a command and the entry contains information associated with a range of addresses and an operation code that are associated with the command [Figures 6 and 7; and paragraphs 0049, 0054 and 0055].

19. As per claim 7, Henderson discloses wherein each entry contains a length and a source address associated with the command [i.e. start of edit and size of edit] [Figure 6; and paragraph 0049].

20. As per claim 9, Henderson discloses wherein the data structure is a table [Figure 7; and paragraph 0007].

21. As per claim 10, Henderson discloses clearing the data structure [i.e. packet context can be cleared] [paragraphs 0039 and 0055].

22. As per claim 11, Henderson discloses wherein the source is a context memory [paragraph 0030].

23. As per claim 13, it is rejected for similar reasons as stated above in claims 1 and 11.

24. As per claim 14, it is rejected for similar reasons as stated above in claim 9.

25. As per claim 15, it is rejected for similar reasons as stated above in claim 4.

26. As per claim 18, it is rejected for similar reasons as stated above in claim 7.

27. As per claim 20, it is rejected for similar reasons as stated above in claim 3.

28. As per claim 21, Henderson discloses wherein the output buffer comprises: data steering logic configured to use the bit mask to identify valid data contained in the transferred packet header data; a working register coupled to the data steering logic and configured to hold the valid packet header data transferred from the data steering logic; and an output queue coupled to the working register and configured to hold the valid packet header data transferred from the working register [Figures 10 and 11; and paragraphs 0041 and 0080-0086].

29. As per claims 22-25, they are rejected for similar reasons as stated above in claims 1-4.

30. As per claims 28-31, they are rejected for similar reasons as stated above in claims 1-4.

31. As per claim 34, it is rejected for similar reasons as stated above in claims 1, 2 and 4. Furthermore, Henderson discloses determining from the entry that the operation is an insert data operation [i.e. insert operation op-code] [608, Figure 6; and paragraph 0049]; and performing the insert data operation, by a device operating independently from the processor, by

determining a leading portion of the packet header data, transferring the leading portion of the packet header data to the output buffer, acquiring insert data, transferring the insert data to the output buffer, determining a lagging portion of the packet header data, and transferring the lagging portion of the packet header data to the output buffer [i.e. using the information from the bit offset, number of bits, operation codes and data fields to perform the desired operation] [602-610, Figure 6; and paragraph 0049].

Claim Rejections - 35 USC § 103

32. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

33. Claims 5, 16, 26, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henderson et al. [US Patent Application No 2004/0042490], in view of Ueno [US Patent Application No 2002/0009050].

34. As per claim 5, Henderson does not specifically disclose the step of: searching the data structure for an entry containing information associated with a range of addresses that matches a range of addresses associated with the acquired packet header data; if a matching entry is found, determining if an operation code contained in the matching entry indicates a delete data operation; and if so, generating a delete bit mask that represents data that is deleted in the

acquired packet header data and transferring the delete bit mask and the acquired packet header data to the output buffer. Ueno discloses the step of: searching the data structure for an entry containing information associated with a range of addresses that matches a range of addresses associated with the acquired packet header data; if a matching entry is found, determining if an operation code contained in the matching entry indicates a delete data operation; and if so, generating a delete bit mask that represents data that is deleted in the acquired packet header data and transferring the delete bit mask and the acquired packet header data to the output buffer [i.e. the label stack deletion or pop operation] [Figures 4 and 5; and paragraphs 0028, 0032, 0033 and 0035]. It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Henderson and Ueno because the teaching of Ueno would enable information or data to be removed correctly to maintain data integrity.

35. As per claims 16, 26 and 32, they are rejected for similar reasons as stated above in claim 5.

36. Claims 8 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henderson et al. [US Patent Application No 2004/0042490], in view of Deforche et al. [US Patent Application No 2005/0232303].

37. As per claim 8, Henderson does not specifically disclose the step of: searching the data

structure for an entry containing information associated with a range of addresses specified by the combination of the length and the source address contained in the entry that matches a range of addresses associated with the acquired packet header data. Deforche discloses the step of: searching the data structure for an entry containing information associated with a range of addresses specified by the combination of the length and the source address contained in the entry that matches a range of addresses associated with the acquired packet header data [paragraphs 0185 and 0186]. It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Henderson and Deforche because the teaching of Deforche would provide a low overhead on processing time and/or low allocation of processing resource [Deforche, paragraphs 0005-0007].

38. As per claim 19, it is rejected for similar reasons as stated above in claim 8.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dustin Nguyen whose telephone number is (571) 272-3971. The examiner can normally be reached on flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached at (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Dustin Nguyen/
Primary Examiner, Art Unit 2454